Simulating spin models on GPU
Lecture 1: GPU architecture and CUDA programming

Martin Weigel

Applied Mathematics Research Centre, Coventry University, Coventry, United Kingdom and
Institut für Physik, Johannes Gutenberg-Universität Mainz, Germany

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traditional interpretation of GPU computing
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Core i7 IvyBridge i7-3870: 122 GFLOP/s
NVIDIA Tesla K10: 4580 GFLOP/s (single precision)
GPU computing

- Core i7 IvyBridge i7-3870: $\approx 21$ GB/s
- NVIDIA Tesla K10: 320 GB/s
Outline

1 Latency vs. throughput
2 GPU architecture
3 Execution model
4 Memory hierarchy
5 CUDA Programming
6 A worked example
7 New in Kepler
CPU vs. GPU hardware

- optimized for low-latency access to cached data
- extensive logic for branch prediction and out-of-order execution
- do an unpredictable scalar job as fast as possible
Latency vs. throughput

CPU vs. GPU hardware

CPU
- optimized for low-latency access to cached data
- extensive logic for branch prediction and out-of-order execution
- do an unpredictable scalar job as fast as possible

GPU
- optimized for data-parallel throughput computations
- latency hiding
- do as many simple, deterministic jobs in parallel as possible
Latency vs. throughput

Latency hiding

**GPU threads**

- **T1**
  - Waiting for data
  - Ready to run
  - Processing

- **T2**
  - Waiting for data
  - Ready to run
  - Processing

- **T3**
  - Waiting for data
  - Ready to run
  - Processing

- **T4**
  - Waiting for data
  - Ready to run
  - Processing

**Legend**

- Red: waiting for data
- Yellow: ready to run
- Green: processing

M. Weigel (Coventry/Mainz)  GPU basics  30/10/2012  6 / 45
Latency hiding

GPU threads

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CPU threads
Latency vs. throughput

Latency hiding

**GPU threads**

- T1
- T2
- T3
- T4

**Legend**

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**CPU threads**

- T1
- T2
- T3

- **CPU** must **minimize latency** of individual thread for responsiveness
- **GPU** *hides latency* through interleaved execution
General processing flow

1. Copy data from host memory to GPU main ("global") memory.
2. Load GPU code, cache data on GPU for performance.
3. Data is persistent in GPU memory, continuous exchange is possible.
4. Copy result from GPU to CPU memory.

M. Weigel (Coventry/Mainz)

GPU basics

30/10/2012
Copy data from host memory to GPU main ("global") memory.
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Load GPU code, cache data on GPU for performance.
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## GPGPU history

### NVIDIA
- introduced CUDA in 2007
- developed into a fully blown ecosystem
- series of computing cards
- academic support programs
  - CUDA professorships
  - CUDA research centers
  - CUDA teaching centers

### ATI
- ATI Stream introduced in 2007
- less viral marketing
- higher peak performance
- somewhat less flexible architecture

### Other architectures
- Intel MIC
  - started as Larabee in 2006
  - prototype board Knight's Ferry (2010)
  - 32 cores with 4 threads/core
  - 2 GB DDR5 memory
- Knight's Corner developed in connection with SGI in 2012
  - more than 50 cores per chip
  - supposedly used in a number of new supercomputers
  - (some) special-purpose machines
- ANTON by D. E. Shaw research, composed of purpose-built ASICs
- Janus, FPGA based machine for spin-model simulations
- QPace, based on the Cell processor known from Playstation 3
- GRAPE, based on FPGAs and used for astrophysical N-body simulations
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Main memory

- up to 8GB in current GPUs
- maximum bandwidth approx. 160 GB/s (Fermi) resp. 320 GB/s (Kepler)
- accessible from CPU and GPU sides
- large latency (see below)
- optional error correction (ECC on/off, Fermi onwards)
GPU architecture: main components

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**Several multiprocessors**
- similar to a multi-core CPU
- each has its own set of registers, scheduler, caches etc.
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Several multiprocessors
- similar to a multi-core CPU
- each has its own set of registers, scheduler, caches etc.
  + scheduling units, PCIe logic etc.

GigaThread scheduler

Interconnect

SM
- Scheduler
- Shared Memory

SM
- Scheduler
- Shared Memory

SM
- Scheduler
- Shared Memory

L2

DRAM
GPU architecture: streaming multiprocessor (Fermi)

**SM components**

- 32 cores per SM (Fermi)
  - 32 fp32 ops/s
  - 16 fp64 ops/s (Tesla)
  - 32 int32 ops/s
- 2 warp schedulers (warp = 32 threads)
  - up to 1536 threads resident in total
- extra special function units (4 for Fermi)
- 64 KB cache on die, re-configurable as 16 KB cache + 32 KB shared memory or vice versa
- 32K 32-bit registers
### GPU architecture: computing core

#### Computing core
- Integer and floating-point units:
  - IEEE-2008 compliant floating point arithmetic (starting from Fermi)
  - Fused multiply-and-add instruction in hardware
- Logic unit
- Move, compare unit
- Branch unit

#### Diagram

![Core diagram](image-url)
NVIDIA GTX 480

- 480 streaming processor cores
- 1.4 GHz clock frequency
- Single precision peak performance 1.3 TFLOP/s
- 1.5 GB GDDR5 RAM
- Memory bandwidth 178 GB/s
GPU computation frameworks

GPGPU = General Purpose Computation on Graphics Processing Unit

“Old” times: use original graphics primitives
- OpenGL
- DirectX

Vendor specific APIs for GPGPU:
- NVIDIA CUDA: library of functions performing computations on GPU (C, C++, Fortran), additional preprocessor with language extensions
- ATI/AMD Stream: similar functionality for ATI GPUs

Device independent schemes:
- BrookGPU (Standford University): compiler for the “Brook stream program language” with backends for different hardware; now merged with AMD Stream
- Sh (University of Waterloo): metaprogramming language for programmable GPUs
- OpenCL (Open Computing Language): open framework for parallel programming across a wide range of devices, ranging from CPUs, Cell processors and GPUs to handheld devices
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Definitions

- **Kernel**: GPU program that runs on a grid of threads
- **Thread**: scalar execution unit
- **Warp**: block of 32 threads executed in lockstep
- **Block**: a set of warps executed on the same SM
- **Grid**: a set of blocks usually executed on different SMs
Threading hierarchy

- Parallel portions of an application are executed on GPU as **kernels**.
  - one kernel is executed at a time (later on modified in concept of **streams**)
  - each kernel executes in many **threads**, but on one **device**
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- Compare CUDA threads to CPU threads
  - CUDA threads are lightweight
    - very little creation overhead
    - low cost of thread switching
  - CUDA needs thousands of threads for efficiency
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    - low cost of thread switching
  - CUDA needs **thousands** of threads for efficiency
- Kernels are executed by an **array** of threads
  - all threads run the same code
  - each thread has a unique **threadid** for control decisions and memory access
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- Kernel launched are in grid of thread blocks
  - threads within block cooperate via shared memory
  - threads within a block can synchronize
  - threads within different blocks cannot cooperate (or only via global memory)
  - block executes on one SM and does not migrate
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  - threads within a block can synchronize
  - threads within different blocks cannot cooperate (or only via global memory)
  - block executes on one SM and does not migrate

- allows programs to transparently scale to GPUs with different numbers of cores
Consider a simple “SAXPY” computation, i.e., “Single-Precision \( A \cdot X + Y \)”. 

**Standard C code**

```c
void saxpy_serial(int n, float a, float *x, float *y) {
    for (int i = 0; i < n; ++i)
        y[i] = a*x[i] + y[i];
}

// Invoke serial SAXPY kernel
saxpy_serial(n, 2.0, x, y);
```

**CUDA C code**

```c
__global__ void saxpy_parallel(int n, float a, float *x, float *y) {
    int i = blockIdx.x*blockDim.x + threadIdx.x;
    if (i < n) y[i] = a*x[i] + y[i];
}

// Invoke parallel SAXPY kernel with 256 threads/block
int nblocks = (n + 255) / 256;
saxpy_parallel<<<nbblocks, 256>>>(n, 2.0, x, y);
```
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Memory hierarchy

Per thread
- Registers (extra fast, no copy for ops)
Memory hierarchy

Per thread

- Registers (extra fast, no copy for ops)
- Local memory
Memory hierarchy

Per thread
- Registers (extra fast, no copy for ops)
- Local memory

Thread blocks: shared memory
- allocated by thread block, same lifetime as block
- allocate as
  ```
  __shared__ int shared_array[DIM];
  ```
- low latency (of the order of 10 cycles), bandwidth up to 1 TB/s
- use for data sharing and user-managed cache

Shared Memory
Memory hierarchy

Per device: global memory

- accessible to all threads on device
- lifetime is user-defined

```c
cuda_malloc(void **pointer, size_t nbytes);
cuda_free(void* pointer);
```

- latency several hundred clock cycles
- bandwidth $\approx 160$ GB/s on Fermi
  (access pattern needs to conform to coalescence rules for good performance)
Memory hierarchy

Per device: global memory

- accessible to all threads on device
- lifetime is user-defined

```c
void *cuda_malloc(void **pointer, size_t nbytes);
void cuda_free(void* pointer);
```

- latency several hundred clock cycles
- bandwidth \( \approx 160 \) GB/s on Fermi (access pattern needs to conform to coalescence rules for good performance)

Per host: device memory

- no direct access from CUDA threads
- copy data to/from device with

```c
void *dest, void *src, size_t nbytes,
```

```c
cudaMemcpyHostToDevice
```

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More generally, the different types of memory have the following characteristics:

<table>
<thead>
<tr>
<th>Memory</th>
<th>Location</th>
<th>Cached</th>
<th>Access</th>
<th>Scope</th>
<th>Lifetime</th>
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<tbody>
<tr>
<td>Register</td>
<td>On-chip</td>
<td>N/A</td>
<td>R/W</td>
<td>One thread</td>
<td>Thread</td>
</tr>
<tr>
<td>Local</td>
<td>Off-chip</td>
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<td>Thread</td>
</tr>
<tr>
<td>Shared</td>
<td>On-chip</td>
<td>N/A</td>
<td>R/W</td>
<td>All threads in a block</td>
<td>Block</td>
</tr>
<tr>
<td>Global</td>
<td>Off-chip</td>
<td>(Yes)</td>
<td>R/W</td>
<td>All threads + host</td>
<td>Application</td>
</tr>
<tr>
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Unified virtual addressing
Unified virtual addressing
GPUDirect 1.0: direct GPU memory access by devices such as network adaptors
GPUDirect 2.0: direct copies from GPU to GPU inside a node
GPUDirect/CUDA 5.0: direct communication between GPUs in different nodes
MPI integration under development
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## CUDA variables

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<td>thread</td>
<td>1X</td>
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<tr>
<td><code>int array_var[10];</code></td>
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<td>100X (pre-Fermi)</td>
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<tr>
<td><code>__shared__ int shared_var;</code></td>
<td>shared</td>
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- automatic scalar variables reside in registers, compiler will spill into local memory in shortage of registers
- automatic array variables (in the absence of qualifiers) reside in thread-local memory
- the type of memory used will be crucial for the performance of the application
Memory allocation

Arrays in device global memory are typically allocated from CPU code. Functions:

- `cudaMalloc(void ** pointer, size_t nbytes);`
- `cudaMemset(void * pointer, int value, size_t count);`
- `cudaFree(void* pointer);`

```c
int n = 1024;
int nbytes = 1024* sizeof(int);
int *a_d = 0;
cudaMalloc( (void**) &a_d, nbytes );
cudaMemset( a_d, 0, nbytes);
cudaFree(a_d);
```
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int *a_d = 0;
cudaMalloc((void**)&a_d, nbytes);
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cudaFree(a_d);
```

The elementary function for data transfers is

- `cudaMemcpy(void *dst, void *src, size_t nbytes, enum cudaMemcpyKind direction);`

  - **direction** is one of `cudaMemcpyHostToDevice`, `cudaMemcpyDeviceToHost` or `cudaMemcpyDeviceToDevice` and specifies location of `src` and `dst`
  - blocks CPU thread (asynchronous transfers possible in streams)
Kernel execution

Function qualifiers

```c
__global__ void f()
```

- function called from host, executed on device
- must return void
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CUDA Programming

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- **__host__ int f()**
  - function called from host, executed on host
  - __host__ and __device__ can be combined to generate CPU and GPU code

**Built-in variables**

All __global__ and __device__ functions have the following automatic variables:

- `dim3 gridDim;` — dimension of the grid in blocks
- `dim3 blockDim;` — dimension of the block in threads
- `dim3 blockIdx;` — block index within grid
- `dim3 threadIdx;` — thread index within block

The indices can be used to construct a global thread index, for instance for a block size of 5 threads,

```
thread_index = blockIdx.x * blockDim.x + threadIdx.x;
```

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\[
\text{thread_index} = \text{blockIdx.x} \times \text{blockDim.x} + \text{threadIdx.x};
\]
**Execution configuration**

Modified C function call syntax:

```c
kernel<<<dim3 dG, dim3 dB>>>(...);
```

Execution configuration:

- **dG**: dimension and size of grid in blocks
  - two-dimensional, \( dG.x \) and \( dG.y \)
  - total number of blocks launched is \( dG.x \times dG.y \)
- **dB**: dimension and size of each block
  - two- or three-dimensional, \( dB.x \), \( dB.y \), and \( dB.z \)
  - total number of threads per block is \( dB.x \times dB.y \times dB.z \)
  - if not specified, \( dB.z = 1 \) is assumed

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The Julia set

**Definition**

Let \( f(z) = p(z)/q(z) \) be a complex function, where \( p(z) \) and \( q(z) \) are complex polynomials.
The Julia set

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The Julia set of $f$ can be described as the set of points for which

$$\lim_{n \to \infty} |f^{(n)}(z)| < \infty,$$

where $f^{(n)}(z)$ denotes the $n$-fold repeated application of $f$ on $z$. 
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In general, the Julia set is a self-similar fractal. Standard example:

\[
f(x) = z^2 + c,
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where \( c \) is a complex constant.
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\]

where \( c \) is a complex constant.

(Color codes are for different rates of divergence.)
A worked example

Julia: CPU code 1

```c
int main ( void ) {
    CPUBitmap bitmap( DIM, DIM );
    unsigned char *ptr = bitmap.get_ptr();

    kernel( ptr );

    bitmap.display_and_exit();
}
```

- CPUBitmap externally defined
- display_and_exit () externally defined
Julia: CPU code 1

**Driver**

```c
int main( void ) {
    CPUBitmap bitmap( DIM, DIM );
    unsigned char *ptr = bitmap.get_ptr();

    kernel( ptr );

    bitmap.display_and_exit();
}
```

**Kernel**

```c
void kernel( unsigned char *ptr ){
for ( int y=0; y<DIM; y++) {
    for ( int x=0; x<DIM; x++) {
        int offset = x + y * DIM;

        int juliaValue = julia( x, y );
        ptr[offset*4 + 0] = 255 * juliaValue;
        ptr[offset*4 + 1] = 0;
        ptr[offset*4 + 2] = 0;
        ptr[offset*4 + 3] = 255;
    }
}
```

- CPUBitmap
  - externally defined
- display_and_exit()
  - externally defined
- julia() will return 1 if point in set
- choose red and black colors, respectively
Julia set function

```c
int julia( int x, int y ) {
    const float scale = 1.5;
    float jx = scale * (float)(DIM/2 - x)/(DIM/2);
    float jy = scale * (float)(DIM/2 - y)/(DIM/2);

    cuComplex c(-0.8, 0.156);
    cuComplex a(jx, jy);

    int i = 0;
    for (i=0; i<200; i++) {
        a = a * a + c;
        if (a.magnitude2() > 1000)
            return 0;
    }

    return 1;
}
```
Julia: CPU code 2

### Julia set function

```c
int julia( int x, int y ) {
    const float scale = 1.5;
    float jx = scale * (float)(DIM/2 - x)/(DIM/2);
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    cuComplex c(-0.8, 0.156);
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    int i = 0;
    for (i=0; i<200; i++) {
        a = a * a + c;
        if (a.magnitude2() > 1000)
            return 0;
    }

    return 1;
}
```

- shift center of image to (0, 0)
- re-scale to unit square in complex plane
- use `scale` factor to zoom
- arbitrary constant `c` in $z_{n+1} = z_n^2 + c$
Data structure

```
struct cuComplex {
  float r;
  float i;
  cuComplex(float a, float b) : r(a), i(b) {}  
  float magnitude2(void) { return r * r + i * i; }
  cuComplex operator*(const cuComplex & a) {
    return cuComplex(r*a.r - i*a.i, i*a.r + r*a.i);
  }
  cuComplex operator+(const cuComplex & a) {
    return cuComplex(r+a.r, i+a.i);
  }
};
```
Data structure

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        return cuComplex(r*a.r - i*a.i, i*a.r + r*a.i);
    }
    cuComplex operator+(const cuComplex& a) {
        return cuComplex(r+a.r, i+a.i);
    }
};
```

- use `cuComplex` structure to represent complex numbers
- operator overloading for natural semantics
int main( void ) {
    DataBlock data;
    CPUBitmap bitmap( DIM, DIM, &data );
    unsigned char * dev_bitmap;

    HANDLE_ERROR( cudaMalloc( (void**) &dev_bitmap, bitmap.image_size() ) );
    data.dev_bitmap = dev_bitmap;

    dim3 grid(DIM,DIM);
    kernel<<<grid,1>>>( dev_bitmap );

    HANDLE_ERROR( cudaMemcpy( bitmap.get_ptr(), dev_bitmap, bitmap.image_size(), cudaMemcpyDeviceToHost ) );

    HANDLE_ERROR( cudaFree( dev_bitmap ) );

    bitmap.display_and_exit();
}
int main( void ) {
    DataBlock data;
    CPUBitmap bitmap( DIM, DIM, &data );
    unsigned char *dev_bitmap;

    HANDLE_ERROR( cudaMalloc( ( void**) & dev_bitmap, bitmap.image_size() ) );
    data.dev_bitmap = dev_bitmap;

    dim3 grid(DIM,DIM);
    kernel<<grid,1>>>( dev_bitmap );

    HANDLE_ERROR( cudaMemcpy( bitmap.get_ptr(), dev_bitmap,
                              bitmap.image_size(),
                              cudaMemcpyDeviceToHost ) );

    HANDLE_ERROR( cudaFree( dev_bitmap ) );

    bitmap.display_and_exit();
}
A worked example

**Julia: GPU code 2**

---

### Kernel

```c
__global__ void kernel( unsigned char *ptr ) {
    // map from blockIdx to pixel position
    int x = blockIdx.x;
    int y = blockIdx.y;
    int offset = x + y * gridDim.x;

    // now calculate the value at that position
    int juliaValue = julia( x, y );
    ptr[offset*4 + 0] = 255 * juliaValue;
    ptr[offset*4 + 1] = 0;
    ptr[offset*4 + 2] = 0;
    ptr[offset*4 + 3] = 255;
}
```
A worked example

Julia: GPU code 2

Kernel

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__global__ void kernel( unsigned char *ptr ) {
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    int x = blockIdx.x;
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    int juliaValue = julia( x, y );
    ptr[offset*4 + 0] = 255 * juliaValue;
    ptr[offset*4 + 1] = 0;
    ptr[offset*4 + 2] = 0;
    ptr[offset*4 + 3] = 255;
}
```

- `__global__` qualifier for device function to be called from host
- each thread gets `threadIdx.x`, `threadIdx.y`, `blockIdx.x`, and `blockIdx.y`
- translate to `offset` in image array
- note that `for` loops have gone away
- four chars to represent R, G, B and alpha channels
Julia function

```c
__device__ int julia( int x, int y ) {
    const float scale = 1.5;
    float jx = scale * (float)(DIM/2 - x)/(DIM/2);
    float jy = scale * (float)(DIM/2 - y)/(DIM/2);

    cuComplex c(-0.8, 0.156);
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    int i = 0;
    for (i=0; i<200; i++) {
        a = a * a + c;
        if (a.magnitude2() > 1000)
            return 0;
    }

    return 1;
}
```
Julia: GPU code 3

Julia function

```c
__device__ int julia( int x, int y ) {
    const float scale = 1.5;
    float jx = scale * ( float )( DIM /2 - x)/( DIM /2);
    float jy = scale * ( float )( DIM /2 - y)/( DIM /2);

    cuComplex c( -0.8, 0.156);
    cuComplex a(jx, jy);

    int i = 0;
    for (i=0; i<200; i++) {
        a = a * a + c;
        if (a.magnitude2() > 1000)
            return 0;
    }

    return 1;
}
```

- `__device__` qualifier for device function to be called from device code
- identical to CPU code apart from function qualifier
**A worked example**

**Julia: GPU code 4**

**Data structure**

```c
struct cuComplex {
    float r;
    float i;
    __device__ cuComplex( float a, float b ) : r(a), i(b) {}
    __device__ float magnitude2( void ) {
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    }
    __device__ cuComplex operator*( const cuComplex& a ) {
        return cuComplex(r*a.r - i*a.i, i*a.r + r*a.i);
    }
    __device__ cuComplex operator+( const cuComplex& a ) {
        return cuComplex(r+a.r, i+a.i);
    }
};
```

Almost identical to CPU version only difference are

__device__ function qualifiers
A worked example

Julia: GPU code 4

Data structure

```c
struct cuComplex {
    float  r;
    float  i;
    __device__ cuComplex( float a, float b ) : r(a), i(b) {}
    __device__ float magnitude2( void ) {
        return r * r + i * i;
    }
    __device__ cuComplex operator *( const cuComplex & a) {
        return cuComplex(r*a.r - i*a.i, i*a.r + r*a.i);
    }
    __device__ cuComplex operator +( const cuComplex & a) {
        return cuComplex(r+a.r, i+a.i);
    }
};
```

- almost identical to CPU version
- only difference are `__device__` function qualifiers
A worked example

Julia: result

Play around with code, cf.

Julia: GPU code — improvements

- On Fermi, maximum number of resident blocks per SM is 8 (16 for Kepler), hence 24 out 32 cores (176 out of 192 for Kepler) are idle.

```c
int x = blockIdx.x*blockDim.x+threadIdx.x;
int y = blockIdx.y*blockDim.y+threadIdx.y;
int offset = x + y * DIM;
if(x >= DIM or y >= DIM ) return ;
```
Julia: GPU code — improvements

- On Fermi, maximum number of resident blocks per SM is 8 (16 for Kepler), hence 24 out of 32 cores (176 out of 192 for Kepler) are idle.

- To improve, one could introduce tiles of, say, $16 \times 16$ pixels with execution configuration:

  ```cu
  dim3 grid((DIM+15)/16,(DIM+15)/16);
  dim3 block(16, 16);
  kernel<<<grid, block>>>( dev_bitmap);
  ```

  and corresponding modification to kernel,

  ```cu
  int x = blockIdx.x*blockDim.x+threadIdx.x;
  int y = blockIdx.y*blockDim.y+threadIdx.y;
  int offset = x + y * DIM;
  if(x >= DIM or y >= DIM) return;
  ```
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  \[
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  \text{dim3 block}(16, 16);
  \text{kernel}<<<\text{grid}, \text{block}>>>( \text{dev_bitmap} );
  \]

  and corresponding modification to kernel,

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  \text{int x = blockIdx.x*blockDim.x+threadIdx.x;}
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  \text{if(x >= DIM or y >= DIM) return;}
  ```

- Could have used virtual unified addressing to eliminate the CPU copy of the image.
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int offset = x + y * DIM;
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```

could have used virtual unified addressing to eliminate the CPU copy of the image.

could integrate with OpenGL for interactive rendering.

...
Outline

1. Latency vs. throughput
2. GPU architecture
3. Execution model
4. Memory hierarchy
5. CUDA Programming
6. A worked example
7. New in Kepler
Extended streaming multiprocessor (SMX)

**Features**
- 192 (instead of 32) cores
- one special function unit per 6 cores (instead of 8)
- maximum number of threads/SM 2048 (instead of 1536)
- 64K 32-bit registers
- 4 warp schedulers
- more flexible shared memory configurations
New in Kepler

- Dynamic parallelism
  - Kernels can more easily generate new threads
  - Kernels can manage associated streams
  - More versatile for recursive algorithms
  - Altogether better load balancing
Hyper-Q

- several work queues allowed to access GPU
- in particular, several CPU threads can access came GPU
- optimized for mixed-type parallelism in MPI clusters
Kepler: further improvements

<table>
<thead>
<tr>
<th>Feature</th>
<th>FERMI GF100</th>
<th>FERMI GF104</th>
<th>KEPLER GK104</th>
<th>KEPLER GK110</th>
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</tr>
<tr>
<td>Dynamic Parallelism</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
</tr>
</tbody>
</table>

- quad-warp scheduler
- warp shuffle instruction
- some features, such as HyperQ and Dynamic Parallelism are disabled in desktop/gaming GPUs!
Summary and outlook

This lecture

This lecture has given a basic introduction into GPGPU and, in particular, the CUDA framework of GPU programming. A basic example has provided a feel for how to go about in using these devices for scientific computing.

Next lecture

In lecture 2, we will start using GPUs for simulating spin models with local algorithms. In terms of GPU programming, a number of additional concepts such as thread synchronization, memory coalescence, and atomic operations will be introduced.

Reading


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